

F142

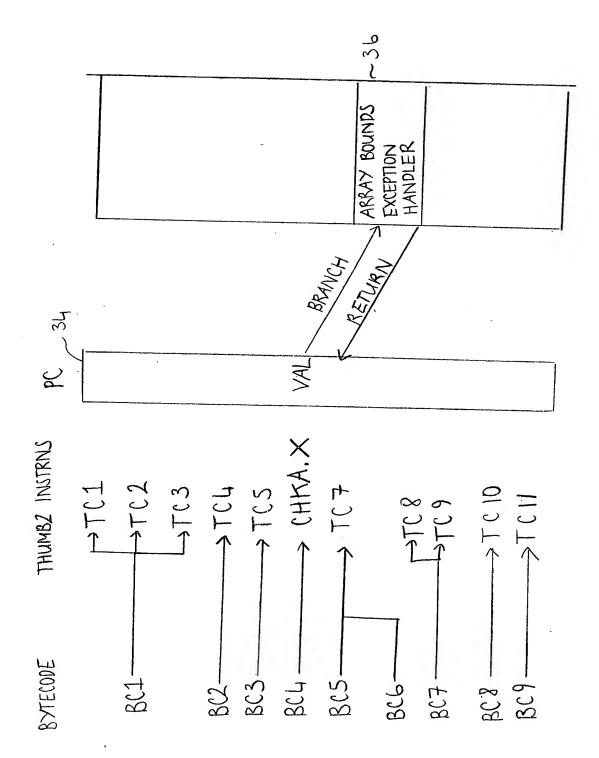


FIG 3

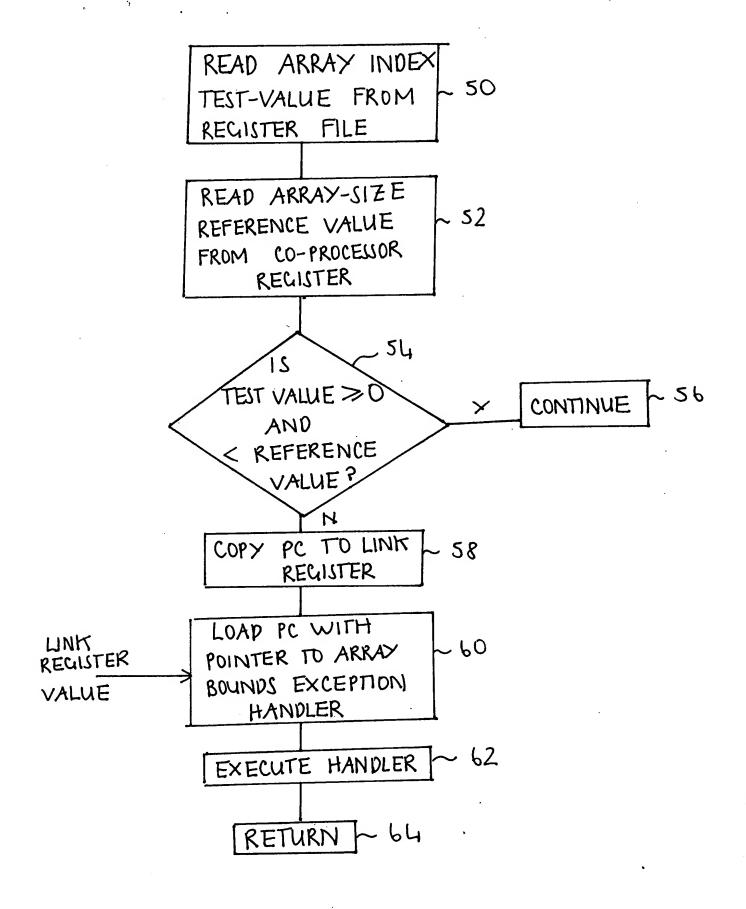


FIG 4

nen the MOV Ir,	·	
not be required when the MOV Ir,	FIGS	

CMP Rn, Rm (16-bit)    15 14 13 12 11 10 9 8 7 6 5	Instruction	ori,	
ding    15	2000		CHKA.X Rn, Rm (16-bit)
CMP Rn, Rm   MOV LS 1r, pc   ADD LS pc, HandlerBase, #-8   H1   H2   Rm   MOV LS 1r, pc   ADD LS pc, HandlerBase, #-8   IndexException   Ir   (unsigned) Rm >= (unsigned) Rn   Ir   pc   HandlerBase, #-8   IndexException   Ir   Expc   Pc   IndexException   Ir   Expc   Ir   Ir   Ir   Ir   Ir   Ir   Ir   I	Encodi	Вu	14 13 12 11 10 9 8 7 6
Ition  It (unsigned) Rm >= (unsigned) Rn.  It = pc  ADD LS pc, HandlerBase, #-8  Ition  It = pc  pc = HandlerBase, #-8; IndexExceptio  pc = HandlerBase, #-8; IndexExceptio  2^N8  This is based upon the CMP(3) 16-bit Thumb-2 instruction that can use high registers  H1 contains the most significant bit for Rn, H2 the most significant bit for Rm  The LS case should almost never occur, so can be treated as exceptional behaviour  This instruction dos not set condition flags  This comparison is UNSIGNED  Return stack prediction will not be required when the MOV is possible in the premited when the most significant premited when the most set the premited when the most set the most set the premited when the most set the premited when the most set the premited when the most set the most set the premited when the most set the			H H2 Rm Rs
It (writion)  ADD 4.5  ADD 4.5  ADD 4.5  ADD 4.5  Ir (writion)  Ir (writ	Thumb	-2 Equivalent	Rn, Rm
Ition  If (urange)  In (urange)			MOVIS 1r,pc
ition  Ir (ur  Jing space  This is based upon the CMP(3) 16-bit Thumb-2 ins H1 contains the most significant bit for Rn, H2 the The L5 case should almost never occur, so can be This instruction dos not set condition flags This comparison is UNSIGNED  Return stack prediction will not be remitted when the			ADD L.S pc, HandlerBase, #-8
Jr.  Jing space  This is based upon the CMP(3) 16-bit Thumb-2 ins H1 contains the most significant bit for Rn, H2 the The L5 case should almost never occur, so can be This instruction dos not set condition flags This comparison is UNSIGNED  Return stack prediction will not be remitted when the	Definiti	uc	<pre>IF (unsigned)Rm &gt;= (unsigned)Rn</pre>
Jing space  This is based upon the CMP(3) 16-bit Thumb-2 ins H1 contains the most significant bit for Rn, H2 the The L5 case should almost never occur, so can be This instruction dos not set condition flags This comparison is UNSIGNED  Return stack prediction will not be remitted when the			1r = pc
This is based upon the CMP(3) 16-bit Thumb-2 ins H1 contains the most significant bit for Rn, H2 the The L5 case should almost never occur, so can be This instruction dos not set condition flags This comparison is UNSIGNED Return stack prediction will not be remitted when the			<pre>pc = HandlerBase, #-8 ; IndexException</pre>
	Encodii	ng space	
	Note	This is based upon the CMP(3) 16-bit Thu	mb-2 instruction that can use high registers
	Note	H1 contains the most significant bit for Rn.	H2 the most significant bit for Rm
	Note	The LS case should almost never occur, s	o can be treated as exceptional behaviour
	Note	This instruction dos not set condition flags	
	Note	This comparison is UNSIGNED	
	Note	Return stack prediction will not be required	when the MOV Ir no step is executed